# Low-Voltage High-Performance Silicon RF Power Transistors

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## Abstract

The high-frequency power performance of mounted discrete silicon bipolar transistors, that have been optimised for low-voltage application, has been evaluated. At 1.8GHz and 3.5V a power gain of 14dB and a power-added efficiency of 60% at an RF power density of 1W/mm emitter length have been measured. These results demonstrate that also at low supply voltages silicon BJTs have excellent power amplifying capabilities.

## Introduction

For portable communication equipment, at 1-2GHz, there is a need for low-voltage, high-performance and cost effective power amplifying devices. At supply voltages of 6V and higher traditionally Si BJTs and NMOS FETs are widely applied. For the next generation of systems, operating at 3V, no preferred technology and/or device architecture has been established. In recent publications, the assumption is made that GaAs MESFET devices will be in favour over Si BJTs, mainly because of higher gain and higher power-added efficiency [1, 2]. However, an objective comparison can be made only if the Si BJT is optimised for low-voltage application. In this paper we will present the power performance of discrete Si bipolar transistors that have been optimised for low-voltage (3V) operation.

## Theory

The most important power figures of a RF power transistor are the output power ($P_{OUT}$), the power gain ($G_P$), the power-added efficiency ($PAE$) and the in- and output impedance. From equivalent-circuit analysis it can be shown that the small-signal power gain of a mounted bipolar transistor in common-emitter configuration can be approximated by (see e.g. [3])

$$G_P = \left(\frac{\omega_T}{\omega}\right)^2 \frac{1}{1+\omega_T R_L C_{BC}} \frac{R_L}{\omega_T L_E + R_E + R_B^*} ,$$

with $R_B^* = R_B(1+\omega_T R_L C_{BC}^{int})$, $\omega_T$ the current-gain cut-off frequency, $R_E$ and $R_B$ the emitter and base series resistance, $L_E$ the emitter grounding inductance, $C_{BC}$ and $C_{BC}^{int}$ the total and internal base-collector capacitance and $R_L$ the load resistance. The above expression is valid under small-signal operation. It is, nevertheless, also useful to estimate qualitatively the influence of transistor and mounting parameters at large-signal class (A)B operation. We have found that for many practical situations the Miller feedback capacitance and the series feedback of the emitter inductance dominate the gain performance of the transistor. ($\omega_T R_L C_{BC} \gg 1$ and $\omega_T L_E \gg R_E + R_B^*$.) Then the power gain is mainly limited by $C_{BC}$ and $L_E$, and the gain expression can be further simplified to

$$G_P \approx \frac{1}{\omega^2} \frac{1}{C_{BC} L_E} \approx \frac{1}{4} \frac{1}{\omega^2} \frac{V_{CE}}{P_{OUT}} \frac{1}{L_E} \frac{I_c^{max}}{C_{BC}} ,$$

in which the approximation $P_{OUT} = I_c^{max} V_{CE}/4$ is used. Consequently, in order to obtain a higher power gain, at given $P_{OUT}$, supply voltage ($V_{CE}$), and packaging technology ($L_E$), the transistor technology must be optimised for maximal collector current over feedback capacitance ratio ($I_c^{max}/C_{BC}$). High $I_c^{max}/C_{BC}$ can be traded off against breakdown voltage by increasing the collector doping level. Minimisation of $C_{BC}$ can be realised by using self-aligned technology to reduce the parasitic base-collector area. Furthermore submicron emitter widths are necessary to prevent current crowding effects and to prevent power gain degradation due to high $R_B$. To realise high power-added efficiency, besides a high power gain (>10dB), the (parasitic) series resistances in the emitter and collector path must be minimal to obtain a low saturation voltage.

## Device Fabrication

To realise these demands self-aligned double-polysilicon bipolar transistors have been fabricated on highly conductive $n^+$ substrates. The device technology is advanced, though not complex, and known from high-



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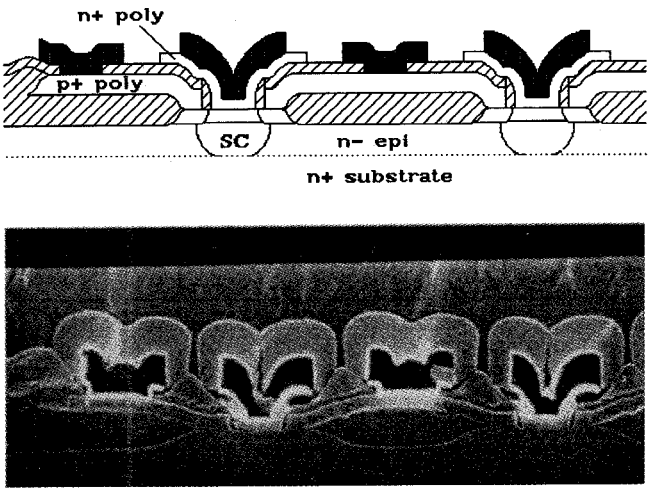


Figure 1: *Schematic (top) and SEM (bottom) cross-section of the double-polysilicon transistor structure used in the experiments.*

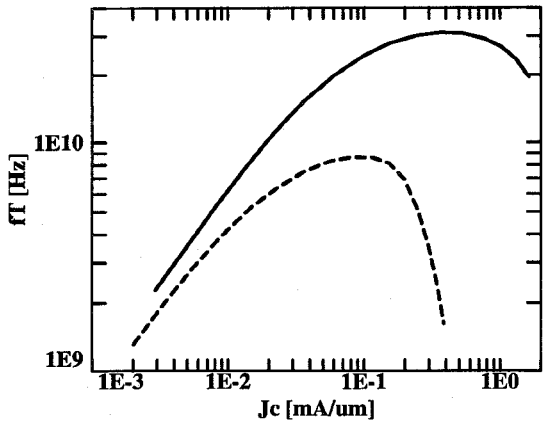


Figure 2: *Cut-off frequency ($f_T$) vs. collector current density for an optimised low-voltage (drawn curve) and a typical conventional 6V (dashed curve) device.*

speed bipolar and BICMOS processing [4]. The device cross-sections of fig. 1 show that the base-collector area of these devices can be minimised, independently of the interconnect metal pitch. As a consequence, minimal $C_{BC}$ can be combined with relaxed metal design rules and a relaxed emitter-emitter pitch to improve the heat spreading capability. To increase $I_c^{max}$ with minimal increase of $C_{BC}$, a selective collector implant (SC) has been applied. The improvement in device performance, in comparison with a typical conventional 6V (non-self-aligned, implanted emitter), microwave transistor, is shown in fig. 2 and table 1.

To evaluate the power performance of this low-voltage, high-frequency bipolar technology, transistors with interdigitated emitter structure (14 emitter fingers with a length of 18$\mu$m) and varying emitter width (from 0.5 to 1.1$\mu$m) have been fabricated.

Table 1: *Comparison of device characteristics.*

| | optimised low-voltage | conventional 6V device |
|---|---|---|
| $f_T^{max}$ [GHz] | 30 | 8 |
| BVCE0 [V] | 4.0 | 10 |
| BVCB0 [V] | 12 | 28 |
| $J_C(f_T^{max})$ [mA/$\mu$m] | 0.4 | 0.1 |
| $\frac{J_C(f_T^{max})}{C_{CB(3V)}}$ [mA/fF] | 0.2 | 0.1 |

## Results and Discussion

For large-signal evaluation the discrete transistor dies have been mounted, collector down, on thin-film $Al_2O_3$ substrates with coplanar transmission line metallisation patterns. Base and emitter have been wire-bonded to the substrate (see fig. 3). The resulting mounting parasitics are comparable with those of standard high-frequency packages ($L_E$=.2nH, $L_B$=.6nH). Low-loss air coplanar wafer probes from Cascade Microtech have been used to connect the device to the test equipment. In this way accurate de-embedding up to the in- and output reference plane of the device can be easily performed and device probing becomes very flexible. The large-signal measurements have been performed using sliding-screw tuners and the source/load pull software package of Maury Microwave [5]. The power measurements have been corrected for system losses and all presented data refers to the in- and output reference plane of the device including bond wires. All measurements were performed under CW and class AB conditions.

In fig. 4 some typical results, at several tuning conditions, are shown. E.g. at 1.8GHz and $V_{CE}$=3.5V an output power of 250mW is obtained at a power gain of 14dB and with a power-added efficiency of 60%. Note that in these devices without ballast resistors, RF power densities up to 2W/mm emitter length have been achieved without thermal problems. Measurements at 0.9GHz resulted in $G_P$=20dB and $PAE$=68% at $P_{OUT}$=250mW. In fig. 5 and table 2 a comparison is made with a conventional 6V device. Both devices were mounted in a simi-

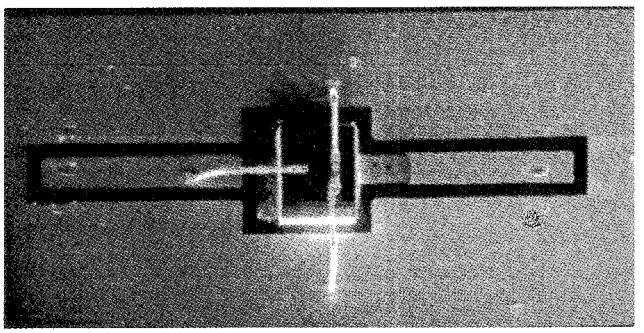

Figure 3: *SEM photograph of a transistor die mounted on a thin film test substrate*

lar way and operated at $V_{CE}$=3.5V. At a given output power the device optimised for low-voltage operation, has about 5dB higher power gain. This improvement in $G_P$ is mainly due to an increase in the $I_c^{max}/C_{BC}$ ratio, but also a higher $f_T^{max}$ and a lower base-emitter capacitance ($C_{BE}$) give some improvement. Note also the significant increase in RF power density and input impedance in favour of the low-voltage device. The high input impedance simplifies interstage impedance matching and therefore the application of these devices. The results clearly show that significant improvement of the power performance of silicon BJTs can be obtained if the technology is optimised for low-voltage application. From fig. 6 it can be seen that the class AB peak $G_P$ increases with decreasing emitter width. This is a result of decreasing $C_{BE}$ and $R_B$. The saturation power however seems independent of the emitter width. This is probably due to current crowding effects in wide emitter devices. Furthermore it has been experimentally observed that wide emitter devices are more sensitive for avalanche and/or thermal induced instabilities.

In fig. 7 it is shown that in a wide range of supply voltages, high gain and efficient operation has been achieved with these devices. Stable operation at a supply voltage in excess of the collector-emitter breakdown (BVCE0=4V) was possible without problems. In addition it was found that, for the shown supply voltage range, the devices are capable of withstanding an output mismatch of VSWR$\leq$10, without any damage.

Finally in fig. 8 measurements are shown of the 2nd and 3rd order harmonic distortion of these high gain devices. As can be seen, distortion levels are well below the carrier power (at 1dB gain compression <-20dBc).

## Conclusions

We have presented the RF power performance of discrete silicon bipolar transistors, that have been optimised for low-voltage high-frequency application. The devices have been fabricated in an advanced, though not complex, technology and were mounted using conventional wire bonding. At 3.5V supply voltage and 1.8GHz a power gain of 14dB and a power-added efficiency of 60% at an RF power density of 1W/mm emitter length was measured for a 250$\mu$m total emitter length device. This is a significant improvement in comparison with a typical conventional Si 6V microwave transistor. Because of their high power gain and high power-added efficiency these low-voltage transistors are ideal devices for portable communication equipment. Consequently, also for low-voltage (3V) applications, Si bipolar transistors remain serious competitors of GaAs MESFET devices.

# References


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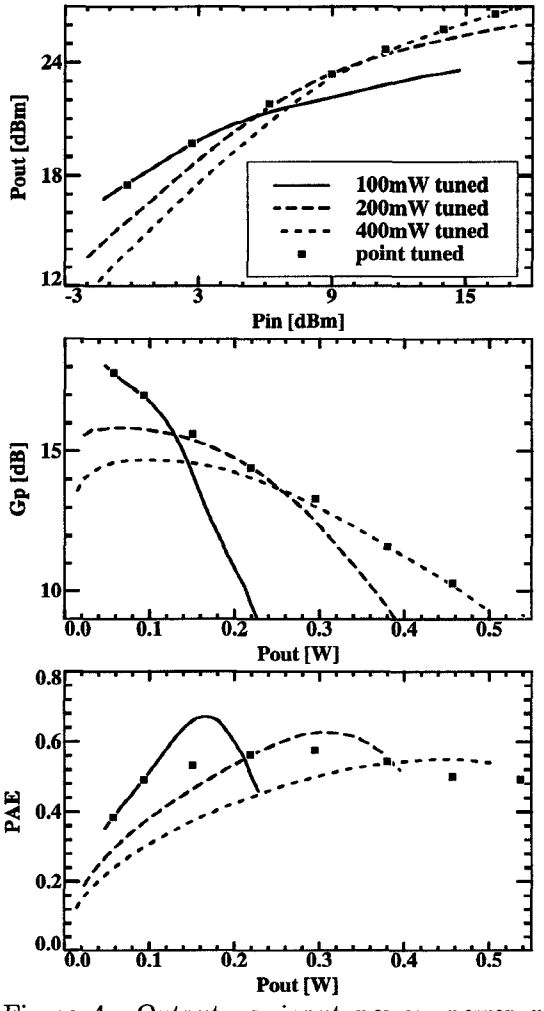


Figure 4: *Output vs. input power, power gain vs. output power and power-added efficiency vs. output power for a 0.5x250(14x18)$\mu m^2$ emitter device at 1.8GHz, $V_{CE}$=3.5V, $V_{BE}$=0.7V and $I_c^{qs}$=0.1mA. Symbols: tuned for maximal power gain. Curves: power sweeps at constant source and load impedance and tuned at power levels as indicated in figure.*

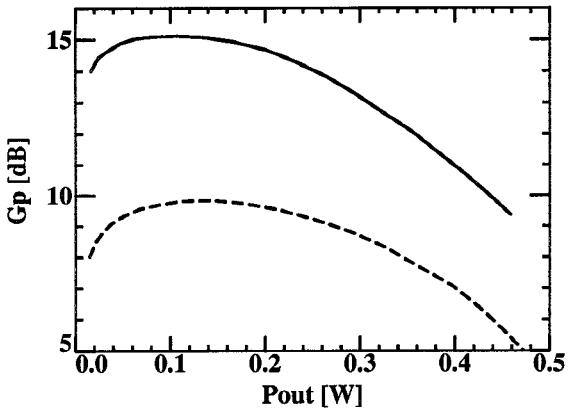


Figure 5: *Power gain vs. output power for an optimised low-voltage (drawn) and a conventional 6V (dashed) device. Both devices operated at 1.8GHz, $V_{CE}$=3.5V and $V_{BE}$=0.7V and tuned around 300mW output power.*

Table 2: *Comparison of power performance at 1.8GHz, $V_{CE}$=3.5V and $V_{BE}$=0.7V.*

| | optimised low-voltage | conventional 6V device |
|---|---|---|
| E width [$\mu$m] | 0.50 | 0.80 |
| E length [$\mu$m] | 250(14x18) | 1500(48x32) |
| $G_P^{max}$ [dB] | 15 | 10 |
| $P_{OUT}(-1dB)$[mW] | 250 | 300 |
| $PAE$(-1dB) [%] | 54 | 55 |
| $Z_{IN}$[$\Omega$] | 12 - j5.0 | 5.0+j3.0 |
| $Z_{LOAD}$[$\Omega$] | 20 + j8.0 | 16+j10 |
| $P_{OUT}$ [mW/$\mu$m] | 1.0 | 0.20 |
| $G_P$ performance bottlenecks | $L_E$ $C_{BC}$ ($f_T$) | $L_E$ $C_{BC}$ $f_T$ |

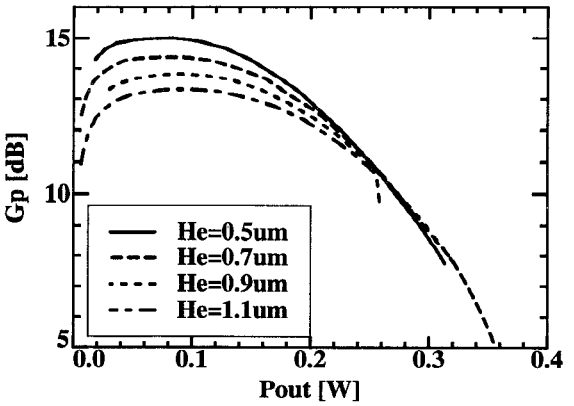


Figure 6: *Influence of emitter width (He) on power gain for 250$\mu$m emitter length devices. f=1.8GHz, $V_{CE}$=3.0V and $V_{BE}$=0.7V. Tuned around 200mW output power.*

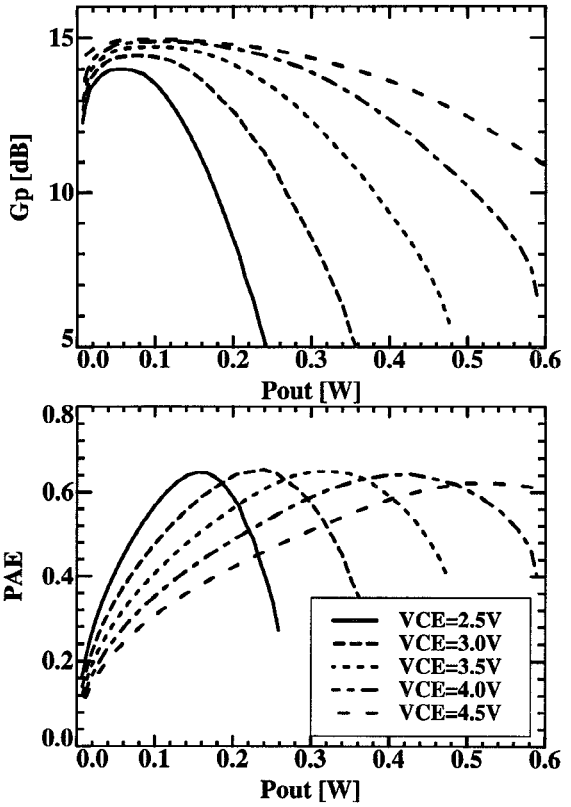


Figure 7: *Influence of supply voltage ($V_{CE}$) on power gain and power-added efficiency for a 0.7x250$\mu m^2$ emitter device at 1.8GHz.*

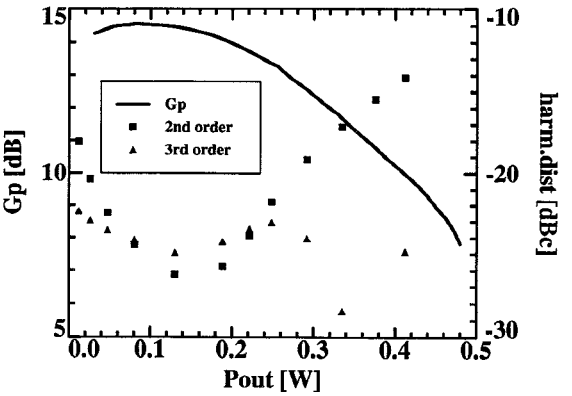


Figure 8: *Power gain and relative harmonic distortion for a 0.7x250$\mu m^2$ emitter device at 1.8GHz and $V_{CE}$=3.5V. Tuned around 250mW output power.*